

FEATURES

- **Audio Input/Output**
 - Up to Three Synchronous Serial Audio Inputs (6 Channels)
 - Up to Two Synchronous Serial Audio Outputs (4 Channels)
 - Left, Right and I²S Input Data Formats: 16-, 20-, or 24-Bit Data
 - Left, Right and I²S Output Data Formats: 16-, 20-, or 24-Bit Data
 - 64 × Fs Bit Clock Rate
 - 24.576-MHz XTAL Input for Master Clock Modes and Clock Auto Detection
 - Slave Mode 256, 384, or 512 × Fs MCLKIN With Automatic Clock Rate Detection
 - Slave Mode 32-, 44.1-, and 48-kHz Fs With Auto Sample Rate Detection
 - Master Mode – 48-kHz Fs 10 Multiplexed Stereo Analog Inputs Selectable Into One Stereo ADC. ADC Maximum Input Level: 1 Vrms SE
 - Three Stereo Differential PWM Outputs
 - High-Quality DNR 100-dBA (Typical) ADC Channel Performance (2 Channels) With Master Mode Clock
 - High-Quality DNR 105-dBA (Typical) PWM Channel Performance (6 Channels)
 - One Single-Ended Analog Stereo Line Driver Output With 1 of 10 Selectable Inputs, 10-kΩ, 100-pF Drive Capability (Maximum Output Level: 1 Vrms)
 - Line-Out Supports Left/Right, Left/Left, and Right/Right Combinations
- **Audio Digital Signal Processor**
 - Programmable Functionality
 - 135-MHz Operation
 - 48-Bit Datapath With 76-Bit Accumulator
 - Hardware Single Cycle Multiplier (28 × 48)
 - Two Memory Loads and One Memory Store Per Cycle
 - Usable 1K Words Data RAM (48 Bit) and Usable 1K Coefficient RAM (28 Bit)
 - 3.25K Words Instruction Program RAM (2.8K Words Available)
 - 360 mS at 48 KHz, 17,408 Words 24-Bit Delay Memory
- **PWM Features**
 - Proven PurePath Digital™ Technology
 - Fourth-Order Chaotic Noise Shaper With Non-Linear Correction
 - High-Quality DNR 105 dBA (Typical) PWM Performance
 - Click and Pop Minimizing at Power Up/Down Using TI Patented Technology
- **General Features**
 - Easy-to-Use Control Interface
 - I²C Serial Control Master and Slave Interface
 - Control Interface Operational Without External MCLK Input
 - Single 3.3-V Power Supply
 - Integrated Regulators
 - 100-Pin TQFP Package
 - M8051 Device Controller
 - Auto Clock and Serial Data Rate Detection and Automatic Device Configuration Without Audible Artifacts

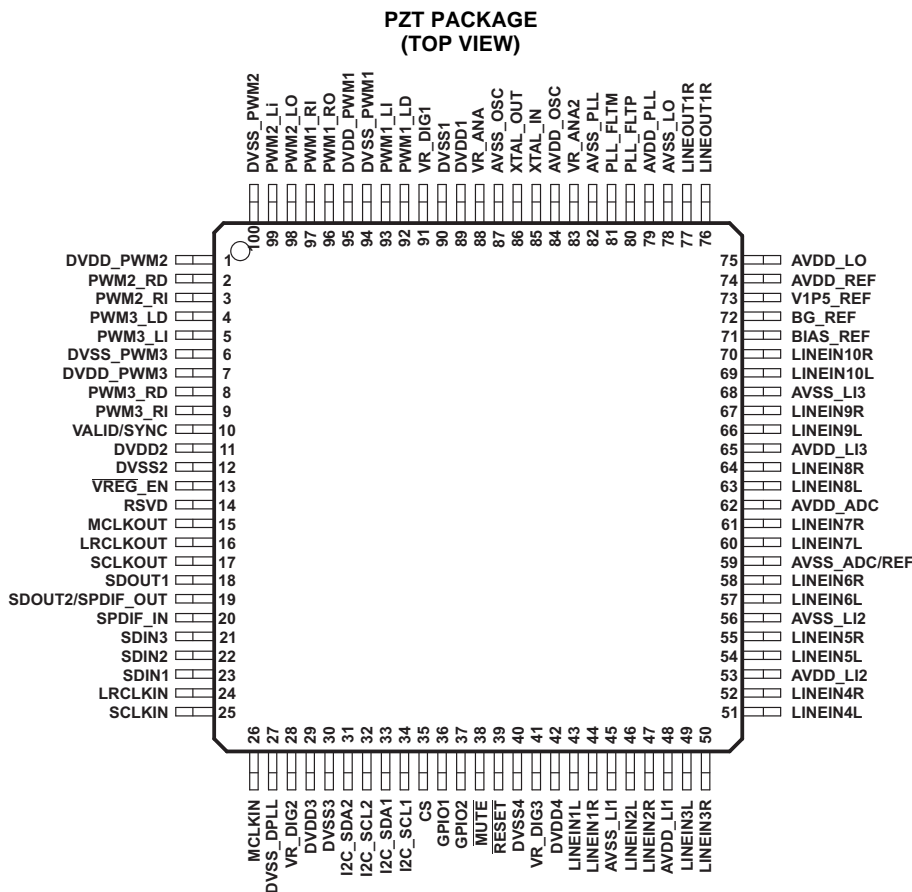


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TAS3308 DIGITAL AUDIO PROCESSOR WITH ANALOG INTERFACE

SLES215A—FEBRUARY 2008—REVISED MARCH 2008



DESCRIPTION/ORDERING INFORMATION

TAS3308 is an audio system-on-a-chip (SOC) designed for digital TV audio systems and mini/micro component applications. It includes analog and digital audio interface. For analog input and output the TAS3308 has ten multiplexed stereo inputs with one stereo ADC and three stereo PWM outputs. For digital input and output the TAS3308 has three I²S inputs and two I²S outputs. One I²S output can also be configured to be S/SPDIF encoded PCM data.

TAS3308 has a programmable audio DSP that preserves high-quality audio by using a 48-bit data path, 28-bit filter coefficients, and a single cycle 28 × 48-bit multiplier. The programmability feature allows users to customize features in the DSP RAM.

ORDERING INFORMATION

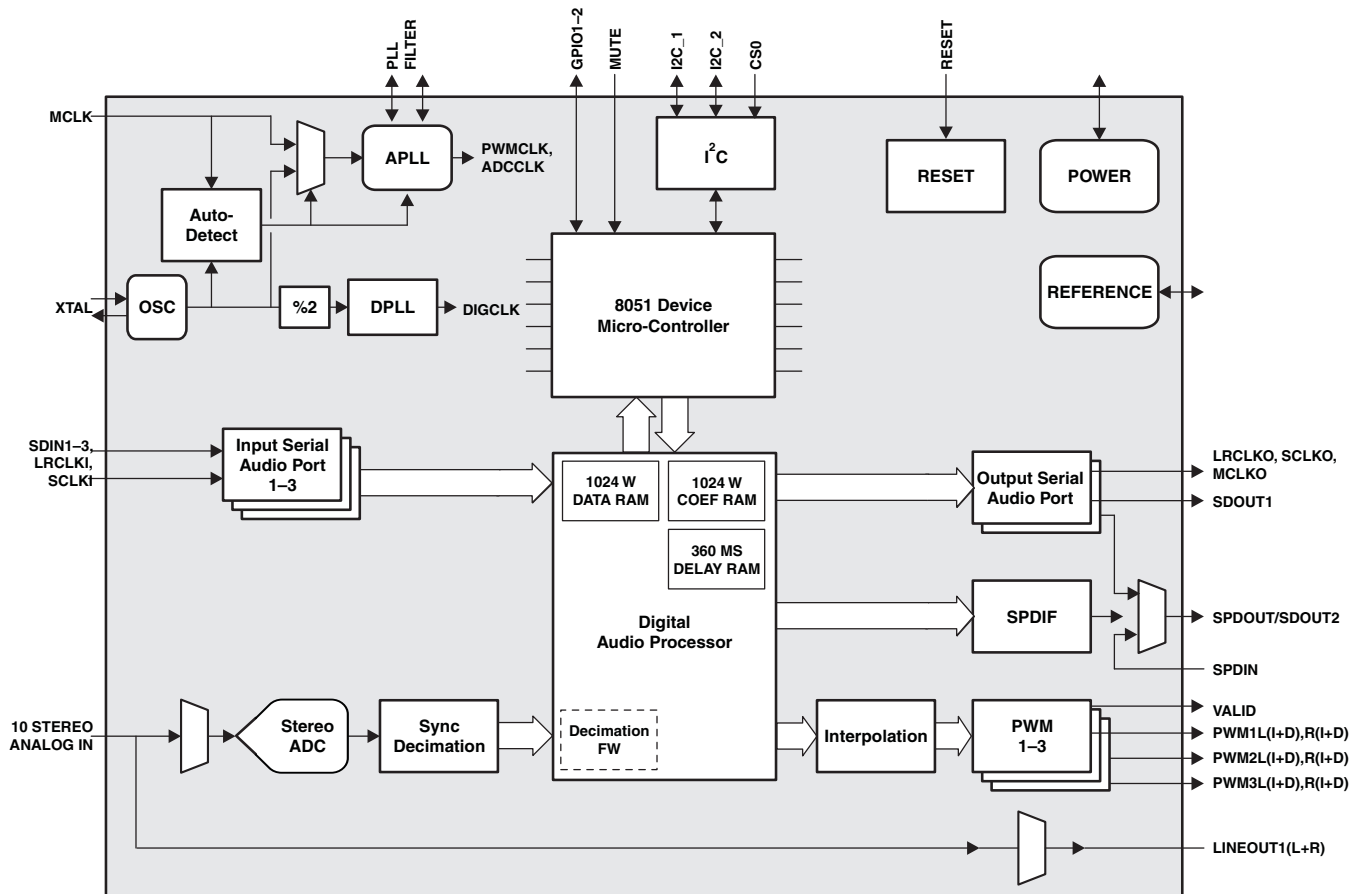
T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PZT	Tray	TAS3308PZT
		Tape and reel	TAS3308PZTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

The TAS3308 comprises nine functional blocks.

- Analog input/MUX/stereo ADC
- Three stereo PWM output for speaker/headphone/stereo
- Line driver outputs
- Clock, digital PLL, analog PLL, serial data interface, and auto-detect system
- Serial control interface/device control
- Audio DSP – digital audio processing
- 8051 device controller
- Power supply
- Internal references

BLOCK DIAGRAM



APPLICATION INFORMATION

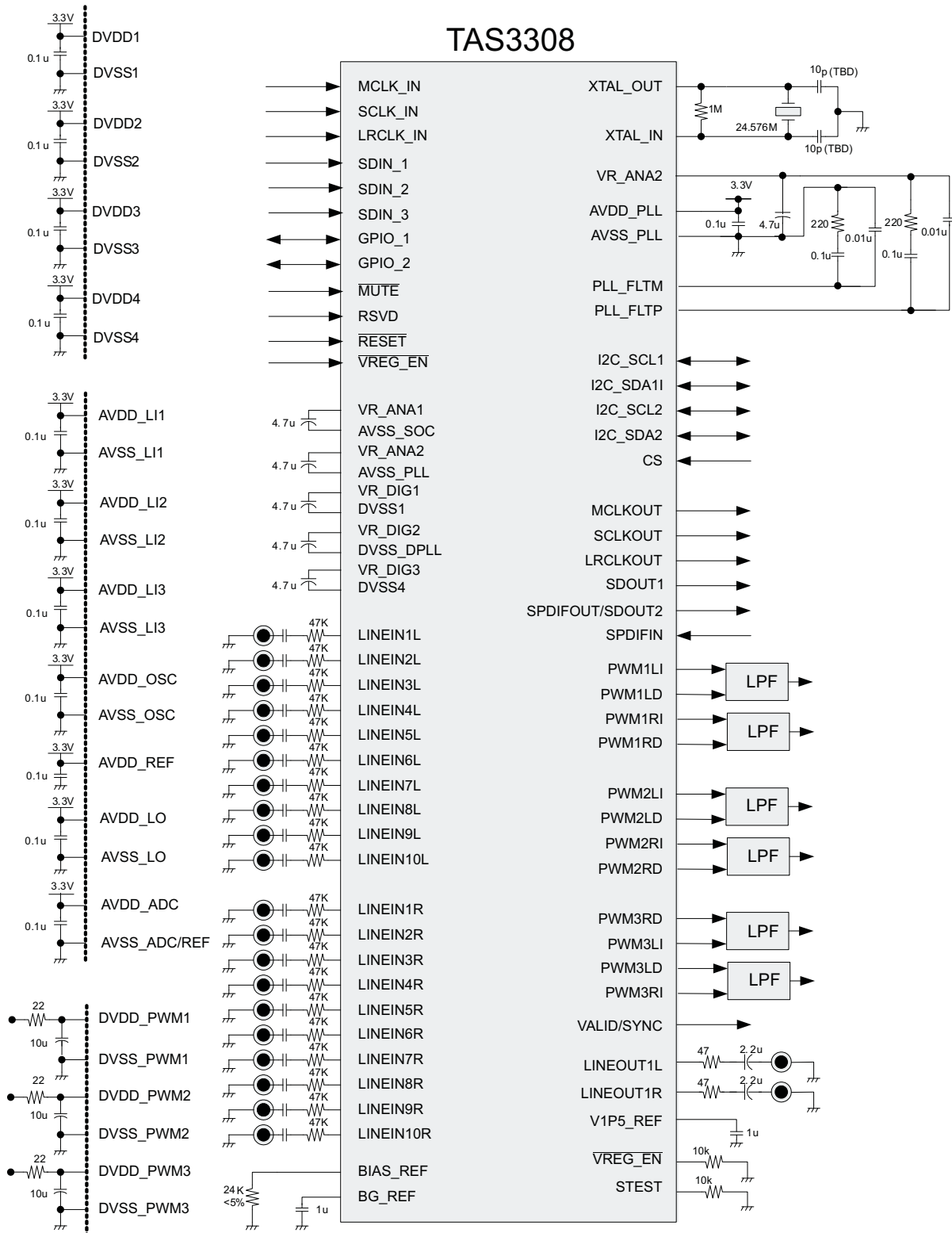


Figure 1. Peripheral Connections

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
DVDD	Supply voltage range		-0.5	3.8	V
AVDD			-0.5	3.8	
DVDD_PWM			-0.5	3.8	
V _I	Input voltage range	3.3 V TTL	-0.5	V _{DD} S + 0.5	V
		3.3 V LVCMOS	-0.5	V _{DD} S + 0.5	
		3.3 V analog	-0.5	AV _{DD} S + 0.5	
		1.8 V LVCMOS	-0.5	AV _{DD} ⁽²⁾ + 0.5	
V _O	Output voltage range	3.3 V TTL	-0.5	V _{DD} S + 0.5	V
		3.3 V LVCMOS	-0.5	V _{DD} S + 0.5	
		3.3 V analog	-0.5	AV _{DD} S + 0.5	
		1.8 V LVCMOS	-0.5	DV _{DD} ⁽³⁾ + 0.5	
			-0.5	AV _{DD} ⁽⁴⁾ + 0.5	
I _{IK}	Input clamp current	V _I < 0 or V _I > DVDD		±20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > DVDD		±20	mA
T _{stg}	Storage temperature range		-65	150	°C
	Lead temperature 1.6 mm (1/16) inch from case for 10 seconds			260	°C

- Stresses beyond those listed under “absolute ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operation conditions” is not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
- AVDD is an internal 1.8-V supply derived from a regulator in the TAS3308 chip. Pin XTALI is the only TAS3308 input that is referenced to this 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTALI.
- DVDD is an internal 1.8-V supply derived from regulators in the TAS3308 chip. DVDD is routed to DVDD_BYPASS_CAP to provide access to external filter capacitors, but should not be used to source power to external devices.
- Pin XTALO is the only TAS3308 output that is derived from the internal 1.8-V logic supply AVDD. The absolute maximum rating listed is for reference; only a crystal should be connected to XTALO. AVDD is also routed to AVDD_BYPASS_CAP to provide access to external filter capacitors, but should not be used to source power to external devices.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASUREMENTS	MIN	NOM	MAX	UNIT
DVDD	Digital supply voltage		3	3.3	3.6	V
AVDD	Analog supply voltage	3.3 V analog	3	3.3	3.6	V
DVDD_PWM	PWM supply voltage	3.3 V PWM	3	3.3	3.6	V
V _{IH}	High-level input voltage	3.3 V TTL	2		V	
		3.3 V LVCMOS (I ² C)	0.7 × V _{DD} S			
		1.8 V LVCMOS (XTL_IN)	1.26			
V _{IL}	Low-level input voltage	3.3 V TTL	0.8		V	
		3.3 V LVCMOS (I ² C)	0	0.3 × V _{DD} S		
		1.8 V LVCMOS (XTL_IN)	0.54			
T _A	Operating ambient air temperature range	(specifying parametrics)	0	25	70	°C
		(specifying functions)	-20	25	70	

TAS3308

DIGITAL AUDIO PROCESSOR WITH ANALOG INTERFACE

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASUREMENT	TEST CONDITIONS	MIN	MAX	UNITS
V _{OH}	High-level output voltage	3.3 V TTL	I _{OH} = -4 mA	2.4		V
		3.3 V LVCMOS (I ² C)	I _{OH} = -0.10 mA	V _{DD5} - 0.2		V
		1.8 V LVCMOS (XTL_OUT)	I _{OH} = -0.6 mA	1.197		V
V _{OL}	Low-level output voltage	3.3 V TTL	I _{OL} = 4 mA		0.5	V
		3.3 V LVCMOS (I ² C)	I _{OL} = 0.10 mA		0.2	V
		1.8 V LVCMOS (XTL_OUT)	I _{OL} = 1.8 mA		0.585	V
I _{OZ}	High-impedance output current	3.3 V TTL			±20	μA
		3.3 V LVCMOS (I ² C)	Driver only, driver disable		±20	μA
I _{IL} ⁽¹⁾	Low-level input current	3.3 V TTL	V _I = V _{IL}		±1	μA
		3.3 V LVCMOS (I ² C)	V _I = V _{IL} , Receiver only		±1	μA
		1.8 V LVCMOS (XTL_IN)	V _I = V _{IL}		±1	μA
I _{IH} ⁽²⁾	High-level input current	1.8 V LVCMOS (XTL_IN)	V _I = V _{IH}		±1	μA
		3.3 V LVCMOS (I ² C)	V _I = V _{IH} , Receiver only		±1	μA
		3.3 V TTL	V _I = V _{IH}		±1	μA
I _{DVDD}	Digital supply current		DSP clock = 135 MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.576 MHz		160	mA
I _{AVDD}	Analog supply current		DSP clock = 135 MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.576 MHz		40	mA
I _{DVDD}	Digital supply current		RESET = LOW		100	mA
I _{AVDD}	Analog supply current		RESET = LOW		10	mA

- (1) Value given is for those input pins that connect to an internal pullup resistor as well as an input buffer. For inputs that have a pulldown resistor or no resistor, I_{IL} is ±1 μA.
- (2) Value given is for those input pins that connect to an internal pulldown resistor as well as an input buffer. For inputs that have a pullup resistor or no resistor, I_{IH} is ±1 μA.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TAS3308PZT	ACTIVE	TQFP	PZT	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS3308PZTR	ACTIVE	TQFP	PZT	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS3308PZTR	TQFP	PZT	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

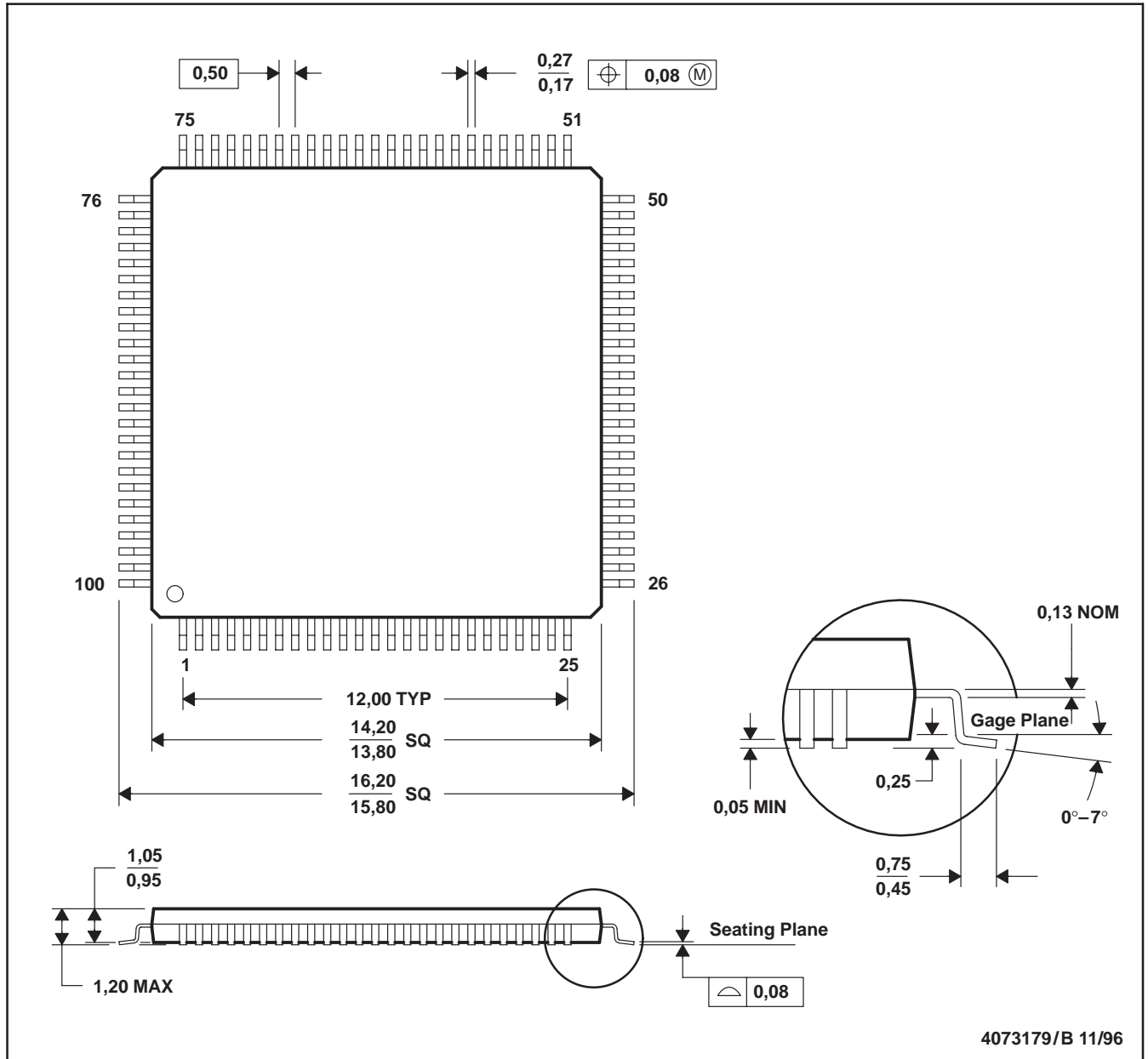


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS3308PZTR	TQFP	PZT	100	1000	346.0	346.0	41.0

PZT (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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